L Number	Hits	Search Text	DB	Time stamp
1	1425	buffer$3 with rate with first with second	USPAT; US-PGPUB; EPO; JPO	2003/10/27 16:00
2	316760	synchroni$5	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:51
3	45	(buffer$3 with rate with first with second) same synchroni$5	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:40
4	47689	detect$3 with synchroni$5	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:45
5	1	(buffer$3 with rate with first with second) same (detect$3 with synchroni$5)	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:44
7	49052	(buffer$3 with rate with first with second) same2 (detect$3 with synchroni$5)	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:44
6	64	(buffer$3 with rate with first with second) and (detect$3 with synchroni$5)	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:44
8	1280	bits with (detect$3 with synchroni$5)	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:46
9	5	(buffer$3 with rate with first with second) and (bits with (detect$3 with synchroni$5))	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:46
10	517	synchroni$5 adj field	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:51
11	1659	sync$10 adj field	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:51
12	0	(buffer$3 with rate with first with second) with (sync$10 adj field)	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:52
13	0	(buffer$3 with rate with first with second) same (sync$10 adj field)	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:52
14	7	(buffer$3 with rate with first with second) and (sync$10 adj field)	USPAT; US-PGPUB; EPO; JPO	2003/10/27 15:52
15	31663	buffer$3 with rate	USPAT; US-PGPUB; EPO; JPO	2003/10/27 16:01
16	41	buffer$3 with (sync$10 adj field)	USPAT; US-PGPUB; EPO; JPO	2003/10/27 16:09
17	14	(buffer$3 with rate) and (buffer$3 with (sync$10 adj field))	USPAT; US-PGPUB; EPO; JPO	2003/10/27 16:02
18	5	rate same (buffer$3 with (sync$10 adj field))	USPAT; US-PGPUB; EPO; JPO	2003/10/27 16:10

US-PAT-NO: 5956377

DOCUMENT-IDENTIFIER: US 5956377 A

TITLE: Method and apparatus for synchronizing frames within a continuous stream of digital data

DATE-ISSUED: September 21, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Lang; Ralph Uwe	Richmond	N/A	N/A	CA

US-CL-CURRENT: 375/372, 370/514 , 375/368

ABSTRACT:

An apparatus is disclosed for synchronizing frames in a continuous stream of digital data consisting of a plurality of master frames (M-bits long) containing data and a constant synchronization word and having an associated bit clock. The apparatus includes a FIFO buffer, a synchronization word register (containing the constant synchronization word) and a comparator operably connected to the FIFO buffer and the synchronization word register to generate a sync detect signal representing whether the portion of the continuous stream of data contained in the FIFO matches the constant synchronization word. The apparatus further includes a frame bit counter controlled by the sync detect signal and the associated bit clock, which generates a frame sync signal every M-bits, a counter connected to a first comparator that generates a sync achieved signal upon the counter output value equaling a first predetermined value and means for incrementing the counter upon coincidence of the sync detect and frame sync signals. The disclosure also discloses a method for synchronizing frames in a continuous stream of digital data while minimizing delay in processing the audio data in a radio communication system including the step of locating a minimized synchronization word in multiple contiguous frames as a predicate to locking synchronization.

2 Claims, 3 Drawing figures

Exemplary Claim Number: 1

Number of Drawing Sheets: 2

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Brief Summary Text - BSTX (14):
In particular, the continuous stream of data is shifted through the FIFO at a rate controlled by the associated bit dock, such that the FIFO buffer holds a portion of the continuous stream at one time. The comparator is operably connected to the FIFO buffer and the synchronization word register, which contains the constant synchronization word. In this arrangement, the comparator or generates a sync detect signal representing whether the portion of the continuous stream of data contained in the FIFO buffer matches the constant synchronization word. The frame bit counter, which is controlled by the associated bit clock, generates a frame sync signal every M-bits. The means for incrementing the counter does so upon coincidence of said sync detect and frame sync signals, such that the counter's output is incremented. This counter output is operably connected to the first comparator, which generates a sync achieved signal upon the counter output value equaling a first predetermined value. In this manner the apparatus can determine appropriate synchronization timing for the continuous stream of digital data, which is indicated by the frame sync signal once the sync achieved signal is generated.

Detailed Description Text - DETX (12):
Upon issuance of RESET, sync channel receiver 200 resets state machine 205 to acquire state (00), as shown in Table 2 at line 1. In the acquire state (00), sync channel receiver 200 scans received digital stream 90 for a first occurrence of SYNC field 110. Scanning is continually performed by FIFO buffer 201, SYNC template register 202 and comparator 203, in combination. SYNC template register 202 contains the preselected synchronization word. Where L is the length of the synchronization word and SYNC template 202, FIFO buffer 201 is a first-in, first-out buffer that is at least L-bits long to facilitate comparison of the received digital stream 90 by comparator 203 between the last L-bits from stream 90 and the L-bit long sync word contained in register 202. In a preferred embodiment, FIFO buffer 201 is implemented by a 1-bit wide, 12-bit long shift-register clocked by a bit rate clock recovered by the

receiver from received digital stream 90, as known in the art. Of course,
other buffering arrangements are within the scope of the present invention.

Detailed Description Text - DETX (19):
In this state, sync channel receiver 200 is waiting for the current master
frame to totally shiftout of FIFO buffer 201 while the next master frame shifts
into position. Like FIFO buffer 201, frame bit counter 204 is docked by the
bit clock recovered from received digital stream 90, such that, as frame bit
counter 204 issues a FRSYN signal, SYNC field 110 should be in FIFO buffer 201
for comparison against SYNC template 202. If the correct SYNC field 110 is
fully in the buffer, comparator 203 issues SDET HIGH. In other words, the
value of SDET 213 (sync detected) "doesn't matter" unless the stream has
advanced M-bits. Inasmuch as FRSYN is LOW, the received digital stream 90 has
not advanced M-bits through FIFO buffer 201, the value of SDET "doesn't
matter." During this time, up/down counter 207 remains at its current value
(LOAD=0 and CE=0).

Detailed Description Text - DETX (22):
At this point in the track state FRSYN is HIGH (indicating the stream has
advanced M-bits), thus, the value of SDET "matters" because SYNC field 110 must
be in the portion of received digital stream 90 in FIFO buffer 201 at this time
if there is any synchronization. In Line 4, SDET is LOW, meaning the SYNC
field 110 was not detected, thus indicating synchronization is off, in turn,
state machine 205 returns to acquire (00) state and reloads up/down counter 207
with "minus 2" (LOAD=1, CE=0 and LOADHIGH=1).

Detailed Description Text - DETX (27):
Although now in lock (11) state, much like Line 3, state machine 205 is
waiting while sync channel receiver 200 merely shifts received digital stream
90 through FIFO buffer 201 looking for the next occurrence of SYNC field 110.
As before, acquisition of SYNC field 110 must also be at the same location in
each master frame 100, so the value of SDET (sync detected) "doesn't matte"
unless the stream has advanced M-bits. In line 7, FRSYN is LOW

indicating that
received digital stream 90 has not advanced M-bits through FIFO buffer 201, so
state machine 205 remains in lock (11) state and up/down counter 207 remains at
its current value (LOAD=0 and CE=0).

Detailed Description Text - DETX (29):
Although FRSYN is HIGH, indicating that FIFO buffer 201 should contain SYNC
field 110, SDET is LOW indicating that no SYNC field 110 is detected, thus in
this instance synchronization is not being correctly tracked by sync channel
receiver 200. In the present invention, any one particular missed sync word
will not necessarily result in a lost synchronization status. Instead, as
explained more fully hereinbelow, state machine 205 in combination with other
elements of sync channel receiver 200 "integrates" these missed sync markers
over time. Accordingly, in response to the missed sync marker, state machine
205 increments up/down counter 207 (LOAD=0, CE=1, UP=1) and continues lock (11)
state.

Claims Text - CLTX (2):
a FIFO buffer through which said continuous stream of data is shifted at a
rate controlled by said associated bit clock, said FIFO buffer holding a
portion of said continuous stream at one time;

Claims Text - CLTX (12):
a FIFO buffer through which said continuous stream of data is shifted at a
rate controlled by said associated bit clock, said FIFO buffer holding a
portion of said continuous stream at a time;